and causes a current to flow in said current mirror circuit connected to said first driver stage.

C1

Claim ~~18~~ 17 (amended). A phase locked loop, comprising:

a phase comparator having a phase comparison circuit with a reference signal input for receiving a reference signal and an input for receiving an input signal whose phase angle is to be regulated, and having a controllable current source circuit according to claim 13 on an output side of said phase comparator;

C2

a loop filter connected to said current source circuit and having an output for outputting an output signal controlling the phase angle of the input signal.

Add the following claims:

--22. The phase locked loop according to claim ~~18~~ 17, wherein said first driver stage of said controllable current source circuit forms a part of a current mirror circuit receiving a flow of a stabilized current when said first driver stage is switched on.--

C3

--23. The phase locked loop according to claim ~~18~~ 17, wherein said current mirror circuit of said controllable current source circuit is coupled to a current mirror circuit

connected to said first driver stage and causes a stabilized current to flow in said current mirror circuit connected to said first driver stage.--

--24. The phase locked loop according to claim 18, wherein a current carried by said first driver stage of said controllable current source circuit when said first driver stage is switched on is greater than a current carried by said second driver stage.--

--25. The phase locked loop according to claim 24, wherein the current carried in said first driver stage of said controllable current source circuit is multiple times greater than the current carried by said second driver stage.--

C3

--26. The phase locked loop according to claim 24, wherein the current carried in said first driver stage of said controllable current source circuit is four times greater than the current carried by said second driver stage.--

--27. The current source circuit according to claim 14, wherein said second driver stage includes:

a circuit node;

a control electrode;

a first and a second current path connected between said supply voltage terminal and said circuit node;

one of said first and said second current paths forming a part of said current mirror circuit connected to said first driver stage; and

C3 a transistor connected between said circuit node and said reference potential terminal, said transistor having a transistor control electrode connected to said control electrode of said second driver stage.--